MPL XEON CLASS SERVER

The MXCS is a highly integrated rugged industrial server available in several specially designed aluminum housings. This allows to operate the MXCS in a moderate or also in a harsh environment. The design integrates standard connectors for easy connection. Therefore the MXCS can be used for any server application where a complete solution is needed.

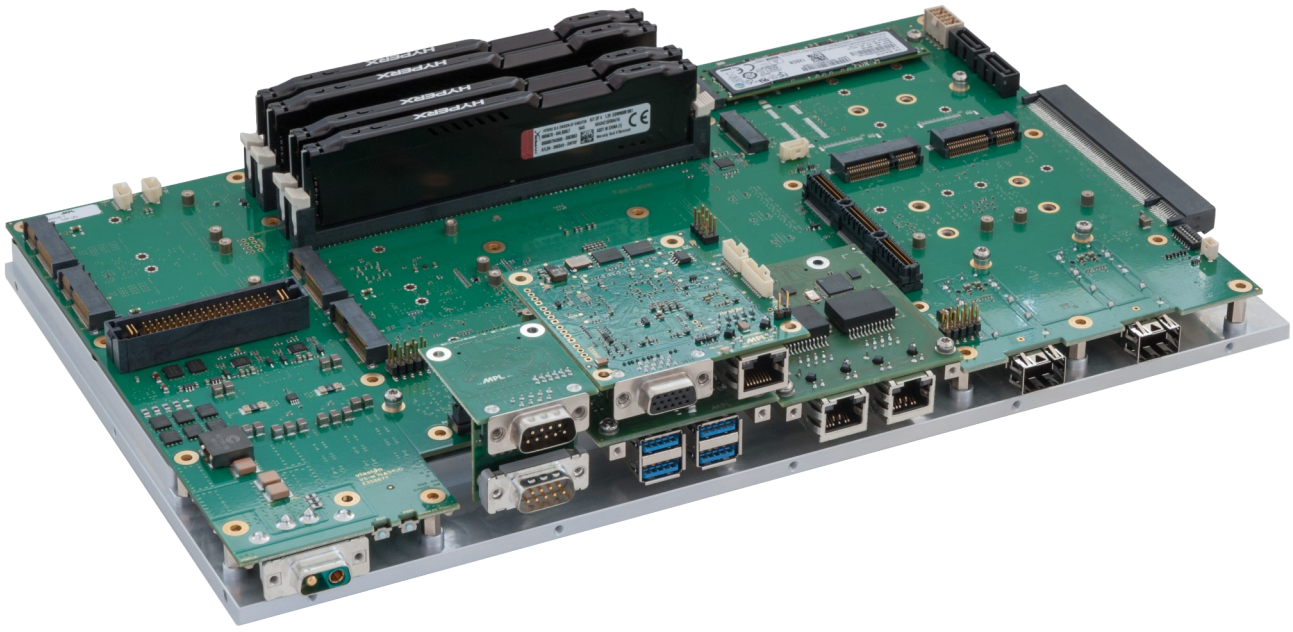
The MXCS housing, available in different sizes, offers space for several add-ons. With the integrated SATA, mSATA and M.2 ports, the PCIe/104 interface, the PCIe x16 lane port and the four PCIe Full-Mini Card sockets there are flexible expansion interfaces available.

Particular precautions have been taken that the entire system EMC is within the CE and FCC limits.

All these features make the MXCS the ideal solution for the industry wherever a flexible, rugged, durable and complete Industrial Server is needed.

Features:

- MXCS-1: Xeon D-1548, 2 GHz, 8 cores with 12 MiB cache, DDR4-2400
- MXCS-2: Xeon D-1587, 1.7 GHz, 16 cores with 24 MiB cache, DDR4-2133
- MXCS-3: Xeon D-1577, 1.3 GHz, 16 cores with 24 MiB cache, DDR4-2133
- Up to 128 GiB dual channel RDIMM memory, or up to 64 GiB dual channel UDIMM memory
- ECC support
- Two SFP+ cages
- Two Intel i210IT 1000Base-T Ethernet ports
- Four USB 3.0 ports (4800 Mbit/s)
- One serial port with RS232 interface
- One serial port with RS232 or RS485 interface
- One VGA graphics port
- One BMC IPMI management port
- One PEG port connector (PCIe x16 Gen3)
- One PCIe/104 Type 1 connector (PCIe x8 Gen3)
- Four mPCIe Full Mini Card sockets
- Two M.2 SATA 3.0 ports (6 Gbit/s)
- Two mSATA 3.0 ports (6 Gbit/s)
- Two standard SATA 3.0 ports (6 Gbit/s)
- Watchdog timer with hardware reset capability
- Power input with load dump and reverse polarity protection
- Reset- and Power Button
- RoHS compliant



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1 INTRODUCTION

1.1 ABOUT THIS MANUAL

This manual and the appropriate MXCS System BIOS User Manual provide information for handling and configuring the MXCS industrial Server. Be sure to read these manuals before attempting to use the MXCS, and keep the manuals close at hand for reference during operation.
This manual is written **for advanced technical personnel** responsible for integrating the MXCS into their systems.
While the Tech Ref Manual and the BIOS User Manual contain deeper information about the MXCS mainboard, contains the Operators Quick Reference Manual an overview about the whole server unit, including the assembled sub modules.

1.2 SAFETY PRECAUTIONS AND HANDLING

For personal safety and safe operation of the MXCS, follow all safety procedures described here and in other sections of the manual.

- Remove power from the system before installing (or removing) the MXCS, to prevent the possibility of personal injury (electrical shock) and / or damage to the product.
- Handle the product carefully; i.e. dropping or mishandling the MXCS can cause damage to assemblies and components.
- Do not expose the equipment to moisture.

1.3 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Various electrical components within the product are sensitive to static and electrostatic discharge. Even a small static discharge can be sufficient to destroy or degrade a component's operation!
Do not touch any electronic components in an open MXCS housing
Handle and mount DIMM modules, PCIe and PCIe/104 cards, mSATA or other add-on modules and also cables to internal connectors only in an ESD protected environment.

1.4 EQUIPMENT SAFETY

Great care is taken by MPL AG that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur.
The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the customers responsibility to protect such equipment when installing this device. MPL AG accepts no responsibility whatsoever for such defects, however caused.

1.5 MANUAL REVISIONS

1.5.1 MANUAL REVISION AND RELATED MXCS VERSIONS

Manual Revision	Related MXCS Versions
A, B	• MXCS-1 rev. A, B, C • MXCS-2 rev. A
C, D	• MXCS-1 rev. D and later • MXCS-2 rev. B and later • MXCS-3 rev. A and later

1.5.2 MANUAL REVISION HISTORY

Manual Revision	Revision Date	Description
A	18.09.2017	• Initial release of this document.
B	22.05.2018	• Temperature range clarified. • Label amended. • Fixed some typos.
C	25.10.2019	• Temperature range with SFP+ support limited to +60°C. • Added new MXCS versions. • Some information clarified. • Added some approved memory and SFP+ modules.
D	19.10.2020	• Fixed some typos. • Added an approved SFP+ module.

1.6 PCB REVISIONS

1.6.1 PCB REVISION AND RELATED MXCS VERSIONS

PCB Revision	Related MXCS Versions
A	• MXCS-1 rev. A, B
B	• MXCS-1 rev. C • MXCS-2 rev. A
C	• MXCS-1 rev. D and later • MXCS-2 rev. B and later • MXCS-3 rev. A and later

1.6.2 PCB REVISION HISTORY

PCB Revision	Description
A	• Prototypes and pre-production samples.
B	• Production models. • LED and Connector markings improved. • TPM module fixation changed to two M2 screws. • 12 V main voltage rail switcher improved. • FAN connector added. • Battery holder changed to an easy release type. • Reset- and power button changed to an easier usable type.
C	• Some changes made to improve producibility. • PCB stackup improved. • Added a power supply temperature protection circuit.

1.7 RELATED DOCUMENTATION

Please note, the MXCS Operators Quick Reference Manual contains information about the whole server unit, including assembled sub modules and used housings. While the MXCS Technical Reference Manual contains deeper information about the MXCS mainboard.
The following documents are related to this manual. For detailed Information about a specific MXCS setting or feature, please see this additional manuals or data sheets.

Reference	Description	Available from	
[1]	MXCS Operators Quick Reference Manual (contains information about the whole server unit)	MPL AG:	www.mpl.ch/t5014.html
[2]	MXCS System BIOS User Manual	MPL AG:	www.mpl.ch/t5014.html
[3]	PCI Express Base Specification 1.1	PCI-SIG:	www.pcisig.com
[4]	PCI Express Base Specification 3.0	PCI-SIG:	www.pcisig.com
[5]	PCI Express CEM Specification 3.0	PCI-SIG:	www.pcisig.com
[6]	PCI Express Mini Card Electromechanical Specification Revision 2.0	PCI-SIG:	www.pcisig.com
[7]	PCI Express M.2 Specification Revision 1.1	PCI-SIG:	www.pcisig.com
[8]	PCIe/104 Specification Version 3.0	PC/104 Embedded Consortium:	www.pc104.org
[9]	Serial ATA Specification Revision 3.1	SATA International Organization:	www.sata-io.org
[10]	Intel Xeon D-1548 CPU data sheet	Intel:	www.intel.com
[11]	Intel Xeon D-1577 CPU data sheet	Intel:	www.intel.com
[12]	Intel Xeon D-1587 CPU data sheet	Intel:	www.intel.com
[13]	Aspeed AST2500 data sheet	Aspeed:	www.aspeedtech.com
[14]	PLX PEX8606 PCIe Switch data sheet	Broadcom:	www.broadcom.com
[15]	Intel i210IT GbE Controller data sheet	Intel:	www.intel.com
[16]	Ti TUSB8041I USB3.0 Hub	Texas Instruments:	www.ti.com
[17]	Microchip USB2514Bi USB2.0 Hub	Microchip:	www.microchip.com
[18]	EXAR XR28V382 data sheet	Exar:	www.exar.com

1.8 STANDARDS COMPLIANCE

The MXCS is designed to meet or exceed the most common industry and military standards. Particular references are:

1.8.1 EMC

- EN 55022 Class B (Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement)
- EN 55024 (Information technology equipment - Immunity characteristics - Limits and methods of measurement)
- EN 61000-4-1 (Electromagnetic compatibility (EMC) -- Part 4-1: Testing and measurement techniques - Overview of IEC 61000-4 series)
- EN 61000-4-2 Level 3, Criterion B (Electromagnetic compatibility (EMC) -- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test)
- EN 61000-4-3 Level 3, Criterion A (Electromagnetic compatibility (EMC) -- Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test)
- EN 61000-4-4 Class 3 (Electromagnetic compatibility (EMC) -- Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test)
- EN 61000-4-5 Class 3 (Electromagnetic compatibility (EMC) -- Part 4-5: Testing and measurement techniques - Surge immunity test)
- EN 61000-4-6 Class 3 (Electromagnetic compatibility (EMC) -- Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields)
- EN 61000-6-1 (Electromagnetic compatibility (EMC) -- Part 6-1: Generic standards - Immunity for residential, commercial and light-industrial environments)
- EN 61000-6-2 (Electromagnetic compatibility (EMC) -- Part 6-2: Generic standards - Immunity for industrial environments)
- EN 61000-6-3 (Electromagnetic compatibility (EMC) -- Part 6-3: Generic standards - Emission standard for residential, commercial and light-industrial environments)
- EN 61000-6-4 (Electromagnetic compatibility (EMC) -- Part 6-4: Generic standards - Emission standard for industrial environments)
- MIL-STD-461E (REQUIREMENTS FOR THE CONTROL OF ELECTROMAGNETIC INTERFERENCE CHARACTERISTICS OF SUBSYSTEMS AND EQUIPMENT)

1.8.2 ENVIRONMENTAL

- EN 50155 (Railway applications - Electronic equipment used on rolling stock)
- MIL-STD-810-F (ENVIRONMENTAL ENGINEERING CONSIDERATIONS AND LABORATORY TESTS)

1.8.3 SAFETY

- EN 60601-1 (Medical electrical equipment -- Part 1: General requirements for safety)
- EN 60950 Class III (Information technology equipment - Safety)

1.8.4 TYPE APPROVAL

- EN 60945 Protected Equipment (Maritime navigation and radiocommunication equipment and systems - General requirements - Methods of testing and required test results)
- E10 (Test Specification for Type Approval)

1.9 MXCS VERSION INFORMATION

The table below gives you an overview of the different MXCS versions and their features.

All MXCS are based on the same MXCS PCB design.

Product Name	Product Features
MXCS-1 MXCS-2 MXCS-3	• MXCS-1: Intel Xeon D-1548, DDR4-2400 • MXCS-2: Intel Xeon D-1587, DDR4-2133 • MXCS-3: Intel Xeon D-1577, DDR4-2133 • 4 DIMM slots supporting up to 4x 16GiB UDIMM or 4x 32 GiB RDIMM modules • Dual channel DDR4-2133 or DDR4-2400 memory bus interface • A high speed Samtec connector with two PCIe interfaces, used for the MXCS Ethernet sub module equipped with two Intel i210IT Ethernet controllers. • A high speed Samtec connector with four USB 3.0 ports, used for the MXCS USB sub module. • A high speed Samtec connector with one LPC bus interface, used for the MXCS Serial Port sub module equipped with the Exar XR28V382 UART used for one RS232 interface, for one optional RS232 or RS485 interface and for the watchdog timer with hardware reset capability. • A high speed Samtec connector with a versatile interface, used for the MXCS IPMI Baseboard Management Controller (BMC) sub module equipped with the AST2500 BMC used for the IPMI management functions and the VGA graphics interface. • Two SFP+ cages • Two SATA 3.0 ports • Two mSATA 3.0 ports • Two M.2 (key M) slots supporting SATA 3.0 • Four mPCIe Full-Mini Card sockets • One PEG Port supporting a x16 lane PCIe Gen3 interface • One PCI/104-Express Type 1 connector supporting a x8 lane PCIe Gen3 interface, two USB 2.0 ports and four x1 lane PCIe Gen2 interfaces • One TPM module port (MPL AG specific pin out) • Suspend to Disk (ACPI S4) support • RoHS compliant
	• Custom assemblies are available for order quantities of 100 units and more. • Please contact MPL AG for further information.
	Please have a look at the MPL AG homepage www.mpl.ch/t5000.html or contact MPL AG for further information.

2 SPECIFICATIONS

2.1 FEATURES SUMMARY

Item	Specifications
SoC	**MXCS-1:** • Intel Xeon D-1548 2 GHz 8-core processor, 12 MByte Cache • DDR4-2400 memory interface **MXCS-2:** • Intel Xeon D-1587 2 GHz 16-core processor, 24 MByte Cache • DDR4-2133 memory interface **MXCS-3:** • Intel Xeon D-1577 2 GHz 16-core processor, 24 MByte Cache • DDR4-2133 memory interface **All:** • Intel Turbo Boost Technology • Intel Hyper-Threading Technology • Intel Virtualization Technology • Intel 64 architecture • Enhanced Intel SpeedStep Technology • Catastrophic thermal protection
Memory	• Dual channel architecture • Four 288 pin DDR4 DIMM sockets support up to 32 GiB RDIMM or 16GiB UDIMM memory modules
Graphics Interfaces	VGA Port: • Available with the MXCS IPMI Baseboard Management Controller (BMC) sub module. • VGA signals support resolutions up to 1920x1200 pixels with 32 bit color at 60 Hz • Aspeed AST2500 graphics controller • ESD protected connector Gen3 PCIe Graphics (PEG) port: • x16 lanes on standard PCIe connector • Supports 3rd party PCIe graphics controller cards
USB	• Available with the MXCS USB sub module • 4 USB 3.0 ports with 1.5/12/480/4800 Mbit/s • Supports USB keyboards and mice as legacy devices • ESD protected connectors
SATA	• 6 SATA 3.0 ports with 6 Gbit/s (2 standard connectors, 2 mSATA slots, 2 M.2 (Key M) slot) • RAID 0/1/5/10 support
1 GbE	• Available with the MXCS Ethernet sub module • 2 Intel i210IT GbE LAN controllers • Each controller resides on a dedicated PCI Express x1 lane link • 9.5 kByte jumbo frame support • Magic Packet Wake on LAN (WOL) support on both interfaces • ESD protected connectors
10 GbE	• Xeon D integrated controller • 2 SFP+ cages • Magic Packet Wake on LAN (WOL) support on both interfaces
Serial Ports	• Available with the MXCS Serial Port sub module with SerifV sub module • 2 full modem RS232 ports on DB9 connectors (16C550 compatible) • 128 bytes FIFO • 1 port optional as RS485 interface available • ESD protected connectors
mPCIe	• 4 mPCIe Full-Mini Card socket with PCIe Gen2 x1 lane link and USB 2.0
PCIe/104 (Type 1)	• 2 USB 2.0 • 4 PCI Express Gen2 x1 lane links • One PCI Express Gen3 x8 lanes link
TPM	• MPL AG specific LPC bus based Trusted Platform Module socket
RTC	• Backed with a field changeable CR2032 battery
Indicator LEDs	• Input power, system power and reset state LEDs

Item	Specifications
RST/PWR Button	• Reset- and Power Button are available at the front plate
Watchdog Timer	• Available with the MXCS Serial Port sub module • XR28V382 UART watchdog timer • Configurable 10 ms, 1 s and 1 minute granularity results in a timeout from 2.5 s up to 4 hours. • Hardware reset capability
Temperature Sensors	• Monitors the CPU and the board temperature
IPMI Interface	• Aspeed AST2500 Baseboard Management Controller (BMC) • 1 Gbit/s LAN Management Port
Power Input	• Load dump protection • Reverse polarity protection

2.2 ELECTRICAL RATINGS

2.2.1 POWER INPUT

Item	Specifications
Input Voltage	• 24 V $^{+50\ \%}/_{-20\ \%}$
Inrush Current	The inrush current depends on parameters that are not MXCS specific, like: • Power supply internal resistance • Power supply voltage rise time and voltage value • Power cable impedance
Protection Circuits	• ESD and EMC protected power input • -36 V_{DC} reverse polarity protection • 150 V load dump protection

2.2.2 POWER DISSIPATION

The power usage changes in a wide range according to the selected MXCS variant, the installation of memory modules or add-on cards and also according to the needed CPU, memory, graphics and interfaces usage. Please find some reference values in the table below:

Power State	MXCS-1 (16GB RAM)	MXCS-2 (128GB RAM)	MXCS-3 (128GB RAM)
ACPI Soft Off, BMC fully booted	7 W	7 W	7W
BIOS Setup Screen	40 W	51 W	47 W
Win7 Desktop Screen w/o CPU Load	24 W	24 W	24 W
Win7 w/ Prime95	63 W	91 W	80 W
Win7 w/ SiSoft Sandra Burn-In Tool	65 W	98 W	76 W

2.3 MECHANICAL SPECIFICATIONS

Item	Specifications
Housing	• Different solutions are available (Desktop, 19“, MIL) • Without ventilation holes
PCB Form Factor	• Length: 330 mm (12.99 inch) • Width: 200 mm (7.87 inch) • Height: Depends on used modules

2.4 ENVIRONMENTAL CONDITIONS

Item	Specifications
Storage Temperature	• -45 °C to +85 °C (-49 °F to +185 °F)
Operating Temperature	• -20 °C to +60 °C (-4 °F to +140 °F) • Optional extended temperature range depends on assembly options, cooling solution and air flow (with SFP+ support maximum 60°C possible).
Relative Humidity	• 5% to 95%, non-condensing
Shock and Vibration	• TBD

3 HARDWARE REFERENCE

3.1 PARTS LOCATION

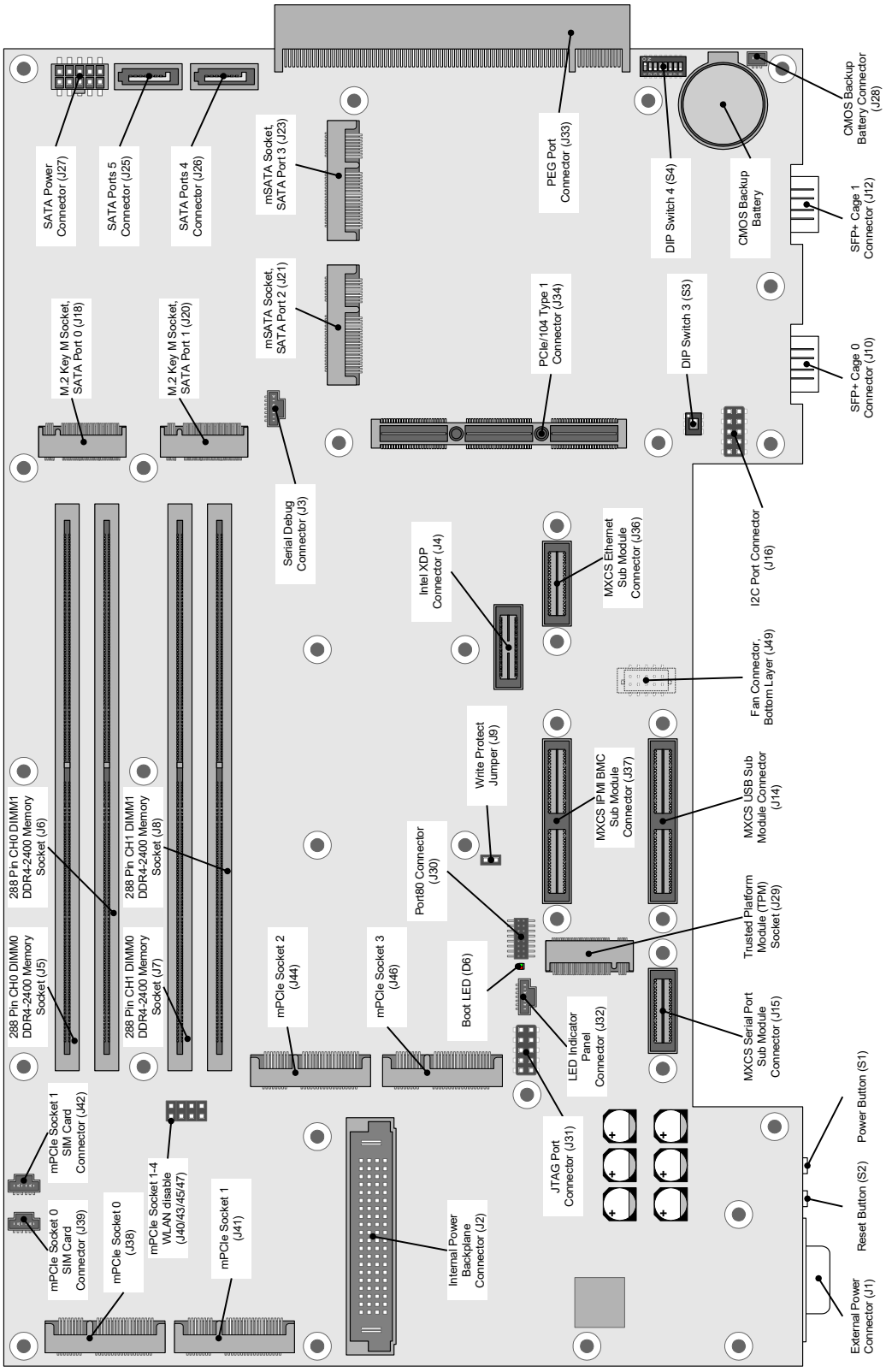


Figure 1: MXCS Parts Location

3.2 SWITCH SETTINGS

3.2.1 PUSH BUTTON 1 (S1) – POWER BUTTON

If pressed an ACPI Power Button event will be triggered.

3.2.2 PUSH BUTTON 2 (S2) – RESET BUTTON

If pressed a System Reset will be triggered.

3.2.3 DIP SWITCH 3 (S3) – RESERVED

This switch is reserved for MPL AG production purpose.

3.2.4 DIP SWITCH 4 (S4) – GENERAL SETTINGS

Default switch settings are in parentheses.

SW2-1	Battery Backup
OFF	CMOS battery backup off
(ON)	CMOS battery backup on
SW2-2	**No Reboot Mode**
(OFF)	Reboot after system failure (TCO Timer system reboot feature enabled)
ON	No Reboot after system failure (TCO Timer system reboot feature disabled)
SW2-3	**Reserved**
(OFF)	Do not use.
ON	
SW2-4	**Reserved**
(OFF)	Do not use.
ON	
SW2-5	**Reserved**
(OFF)	Do not use.
ON	
SW2-6	**Reserved**
(OFF)	Do not use.
ON	
SW2-7	**Ethernet Controller 2 Disable**
(OFF)	Ethernet Controller 2 enabled
ON	Ethernet Controller 2 disabled
SW2-8	**Ethernet Controller 1 Disable**
(OFF)	Ethernet Controller 1 enabled
ON	Ethernet Controller 1 disabled

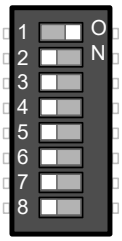


Figure 2: DIP Switch 4

3.3 CONNECTORS

3.3.1 EXTERNAL CONNECTORS

All the external interface connectors are supplied via additional MXCS sub modules. Available sub modules are:

- MXCS IPMI Baseboard Management Controller (BMC) sub module
- MXCS Serial Port sub module with SerifV sub module
- MXCS USB sub module
- MXCS Ethernet sub module

3.3.1.1 External Power Connector (J1)

3.3.1.1.1 Pin Assignment

The external power connector counterpart is: Conec 302W2CPXX99A10X with solder contacts Conec 132C10029X and 131C10029X and with shell FCI 8655MH0901BLF.

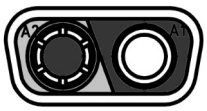
Pin	Signal	Description	Pin Assignment
A1	VIN_CON	Input Power + (24 $V_{NOMINAL}$)	
A2	GND_CON	Input Power – (0 V), connected to Case EARTH	

Figure 3: Power Connector (Conec, 302W2CSXX56N40X)

3.3.1.1.2 Power Input Protection Circuits

Item	Specifications
Reverse polarity protection	-36 V
Load dump protection	+150 V

The MXCS includes a reverse polarity protection up to the reverse maximum supply voltage. If this condition occurs, switch the power supply off, connect it correctly, turn it on again and power up the MXCS.
The load dump protection circuit cuts the supply voltage to 36 V. To avoid an overheat condition in the load dump protection circuit, the MXCS immediately shuts down, if the over voltage (> 36 V) is applied longer than ~5 ms.

3.3.1.1.3 Power Up Behavior

A voltage greater than ~8 V between VIN_CON and GND_CON, lets the MXCS boot. If the MXCS was shut down with the OS functionality or with a Power Button Override (push the Power Button 4 seconds), you have to start the MXCS with a short activation of the Power Button, or you can cycle VIN_CON.
For a proper power up, there is a 5 s timeout included between a power down and an immediately following power up cycle.

3.3.1.2 Serial Port Connector

This connector supports a standard RS232 interface. It is available with the MXCS Serial Port sub module.

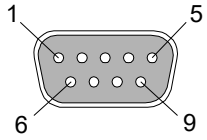
Pin	Signal	Description	Pin Assignment
1	DCD	Carrier detect	
2	RXDn	Receive data	
3	TXDn	Transmit data	
4	DTR	Data terminal ready	
5	GND	Ground	
6	DSR	Data set ready	
7	RTS	Request to send	
8	CTS	Clear to send	
9	RI	Ring indicator	

Figure 4: Serial Port Connector (DSUB 9 Male) (Compona, 363 011-0)

3.3.1.3 Optional 2nd Serial Port Connector

This connector is only available if a SerifV-1 (RS232) or SerifV-2 (RS485) module in combination with the MXCS Serial Port sub module is used.
The Ring Indicator (RI) wake up from ATX Power State S5 (Soft Off) is not available at this port.

With RS232 Module (SerifV-1)			Pin Assignment
Pin	**Signal**	**Description**	
1	DCD	Carrier detect	
2	RXDn	Receive data	
3	TXDn	Transmit data	
4	DTR	Data terminal ready	
5	GND	Ground	
6	DSR	Data set ready	
7	RTS	Request to send	
8	CTS	Clear to send	
9	RI	Ring indicator	
With RS485 Module (SerifV-2)			
Pin	**Signal**	**Description**	
1	NC	Not connected	
2	Rx+	Receive data +	
3	Tx+	Transmit data +	
4	NC	Not connected	
5	GND_isolate	Galvanically isolated Ground	
6	NC	Not connected	
7	Rx-	Receive data -	
8	Tx-	Transmit data -	
9	NC	Not connected	

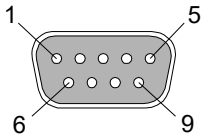


Figure 5: Serial Port Connector (DSUB 9 Male) (Compona, 329 351-5)

3.3.1.4 Dual USB 3.0 Connectors

These connectors support four USB 3.0 Low-, Full-, Hi- and SuperSpeed interfaces. They are available with the MXCS USB sub module.

Pin	Signal	Description	Pin Assignment
1	VCC0/2	Port 0/2 Cable Power +5 V	
2	P0/2-	Port 0/2 Balanced Data Line -	
3	P0/2+	Port 0/2 Balanced Data Line +	
4	GND0/2	Port 0/2 Cable Ground	
5	USB30_RX0/2-	USB3.0 Port 0/2 Receive -	
6	USB30_RX0/2+	USB3.0 Port 0/2 Receive +	
7	GND0/2	Port 0/2 Cable Ground	
8	USB30_TX0/2-	USB3.0 Port 0/2 Transmit -	
9	USB30_TX0/2+	USB3.0 Port 0/2 Transmit +	
10	VCC1/3	Port 1/3 Cable Power +5 V	
11	P1/3-	Port 1/3 Balanced Data Line -	
12	P1/3+	Port 1/3 Balanced Data Line +	
13	GND1/3	Port 1/3 Cable Ground	
14	USB30_RX1/3-	USB3.0 Port 1/3 Receive -	
15	USB30_RX1/3+	USB3.0 Port 1/3 Receive +	
16	GND1/3	Port 1/3 Cable Ground	
17	USB30_TX1/3-	USB3.0 Port 1/3 Transmit -	
18	USB30_TX1/3+	USB3.0 Port 1/3 Transmit +	

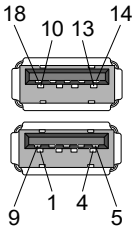


Figure 6: Dual USB 3.0 (Type A) Connector (TE, 1932355-1)

3.3.1.5 VGA Connector

VGA connector with legacy analog port. It is available with the MXCS IPMI Baseboard Management Controller (BMC) sub module.

Pin	Signal Description	Pin Assignment
1	Analog Red	
2	Analog Green	
3	Analog Blue	
4	NC	
5	Ground	
6	Analog Ground	
7	Analog Ground	
8	Analog Ground	
9	+5 V VGA Power	
10	Ground	
11	NC	
12	DDC Data	
13	Analog Horizontal Sync	
14	Analog Vertical Sync	
15	DDC Clock	

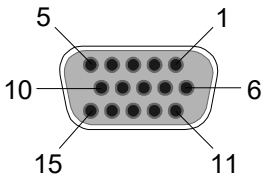


Figure 7: VGA Connector (Compona, 363062)

3.3.1.6 IPMI Management Port 1000Base-T Ethernet Connector

Standard RJ45 connector. It is available with the MXCS IPMI Baseboard Management Controller (BMC) sub module.

Pin	Signal	Description	Pin Assignment
1	TD0+	Data 0 +	
2	TD0-	Data 0 -	
3	TD1+	Data 1 +	
4	TD2+	Data 2 +	
5	TD2-	Data 2 -	
6	TD1-	Data 1 -	
7	TD3+	Data 3 +	
8	TD3-	Data 3 -	

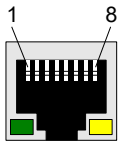


Figure 8: RJ45 Connector (HanRun, HR921148C)

3.3.1.7 1000Base-T Ethernet Connectors

Standard RJ45 connectors. They are available with the MXCS Ethernet sub module.

Pin	Signal	Description	Pin Assignment
1	TD0+	Data 0 +	
2	TD0-	Data 0 -	
3	TD1+	Data 1 +	
4	TD2+	Data 2 +	
5	TD2-	Data 2 -	
6	TD1-	Data 1 -	
7	TD3+	Data 3 +	
8	TD3-	Data 3 -	

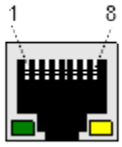


Figure 9: RJ45 Connector (Steward, SS-7488SC5-CC-PG4-BA-A403)

3.3.1.8 SFP+ Cage Connectors (J10, J12)

These are SFP+ cages, which conform to the Small Form-Factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA) INF-8074i specification and support 10 Gbit/s data rate.

Pin	Signal	Description	Pin Assignment
1	VeeT	Transmitter Ground	
2	TX Fault	Transmitter Fault Indication	
3	TX Disable	Transmitter Disable	
4	MOD-DEF2 / SDA	Module Definition 2, Serial ID Data	
5	MOD-DEF1 / SCL	Module Definition 1, Serial ID Clock	
6	MOD-DEF0 / ABS	Module Definition 0	
7	Rate-Sel	Select Receiver Bandwidth	
8	LOS	Loss of Signal	
9	VeeR	Receiver Ground	
10	VeeR	Receiver Ground	
11	VeeR	Receiver Ground	
12	RX -	Received Data Out Inverted	
13	RX +	Received Data Out	
14	VeeR	Receiver Ground	
15	VccR	Receiver Power	
16	VccT	Transmitter Power	
17	VeeT	Transmitter Ground	
18	TX +	Transmit Data In	
19	TX -	Transmit Data In Inverted	
20	VeeT	Transmitter Ground	

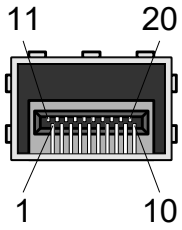


Figure 10: SFP+ Cage Connector ((Samtec, MECT-110-01-M-D-RA1 and SFPC-SL)

3.3.2 INTERNAL CONNECTORS

3.3.2.1 Internal Power Backplane Connector (J2)

Shrouded 2 mm header with high current contacts.

Pin	Signal	Description
P1, P2, A10, A12, A14, A16, A18, A20, B11, B13, B15, B17, B19, B9, C10, C12, C14, C16, C18, C20, C3, C7, D11, D13, D15, D17, D19, D6, D9	GND	Ground
A1, C1	VEE_PoE	PoE Negative Supply
B1, D1	GND_PoE	PoE Positive Supply
A2, B2, C2, C8, D2	NC	Not Connected
A3	SYSPWROK	System Power OK
A4	PLTRSTn	Platform Reset
A5	SLP_S3n	Sleep S3 Signal
A6	LED_DATAn	LED Bus Data
A7	LED_GATE	LED Bus Gate
A8	LED_CLOCK	LED Bus Clock
A9, C9, A11, B12, C11, D10, D12	+12V_SB	+12 V Standby Voltage
A13, A15, B14, B16, C13, C15, D14, D16	VIN_UPS	UPS Input Voltage
A17, A19, B18, B20, C17, C19, D18, D20	VIN_FLT	Input Power positive Voltage
B3	PWROKn_VIN1	V_{IN1} Power OK
B4	PWROKN_VIN2	V_{IN2} Power OK
B5	PWROKN_VIN3	V_{IN3} Power OK
B6	PRESENTn_VIN1	V_{IN1} Power Present
B7	PRESENTn_VIN2	V_{IN2} Power Present
B8	PRESENTn_VIN3	V_{IN3} Power Present
B10	+2.5-5.0V_BAT	+2.5 .. +5 V CMOS Battery Voltage
C4	RSTBTNn	Reset Button
C5	PWRBTNn	Power Button
C6	IGNITION	Ignition Signal
D3	+5.0V	+5 V System Voltage
D4	USB20_p	USB Port Balanced Data Line +
D5	USB20_n	USB Port Balanced Data Line -
D7	+5.0V_SB	+5 V Standby Voltage
D8	+3.3V_SB	+3.3 V Standby Voltage

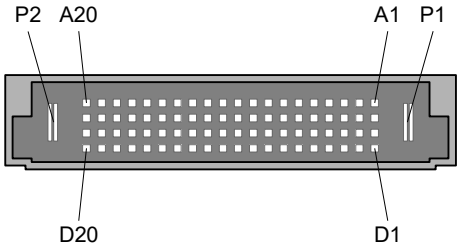


Figure 11: Internal Power Backplane Connector (Samtec, MPTC-01-80-01-LC)

3.3.2.2 M.2 Module Socket (J18, J20)

These sockets support M.2 modules (Key M) with SATA Gen 3.0 interface with up to 600 MB/s data transfer rate.

Pin	Signal	Signal Description	Pin Assignment
1, 3, 9, 15, 21, 27, 33, 39, 45, 51, 57, 71, 73, 75	GND	System Ground	
2, 4, 12, 14, 16, 18, 70, 72, 74	+3.3V	+3.3 V System Voltage	
5, 6, 7, 8, 11, 13, 17, 19, 20, 22, 23, 24, 25, 26, 28, 29, 30, 31, 32, 34, 35, 36, 37, 40, 42, 44, 46, 48, 50, 52, 53, 54, 55, 56, 58, 67, 69	NC	Not Connected	
10	NC (LED1n)	Not Connected	
38	GND (DEVSLP)	System Ground	
41, 43	SATA_RX0/1p/n	SATA 3.0 Port 0/1 Receive	
49, 47	SATA_TX0/1p/n	SATA 3.0 Port 0/1 Transmit	
68	GND (SUSCLK)	System Ground	

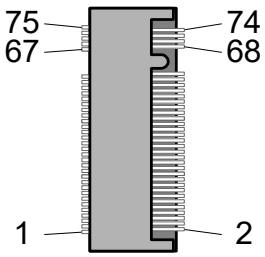


Figure 12: M.2 Key M Socket Connector (TE, TE12199230-6)

3.3.2.3 mSATA Full-Mini Card Sockets (J21, J23)

These sockets support mSATA Full-Mini Card modules according to Serial ATA Specification Revision 3.1 with up to 600 MB/s data transfer rate.

Pin	Signal	Pin	Signal	Pin Assignment
1	Not Connected	2	+3.3V	
3	Not Connected	4	GND	
5	Not Connected	6	+1.5V	
7	Not Connected	8	Not Connected	
9	GND	10	Not Connected	
11	Not Connected	12	Not Connected	
13	Not Connected	14	Not Connected	
15	GND	16	Not Connected	
17	Not Connected	18	GND	
19	Not Connected	20	Not Connected	
21	GND (CARD_DETECTn)	22	Not Connected	
23	SATA_RX2/3p	24	+3.3V	
25	SATA_RX2/3n	26	GND	
27	GND	28	+1.5V	
29	GND	30	Not Connected	
31	SATA_TX2/3n	32	Not Connected	
33	SATA_TX2/3p	34	GND	
35	GND	36	Not Connected	
37	GND	38	Not Connected	
39	+3.3V	40	GND	
41	+3.3V	42	Not Connected	
43	GND (mSATA_SELECT)	44	Not Connected	
45	Not Connected	46	Not Connected	
47	Not Connected	48	+1.5V	
49	Not Connected	50	GND	
51	Not Connected	52	+3.3V	

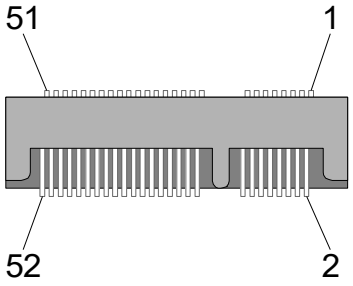


Figure 13: mSATA Full-Mini Card Socket Connector (JAE, MM60-52B1-E1-R650)

3.3.2.4 Trusted Platform Module (TPM) Socket (J29)

This connector is reserved for future MPL AG system expansions.

Pin	Signal	Signal Description	Pin Assignment
1, 3, 9, 15, 21, 27, 33, 39, 45, 51, 52, 53, 57, 71, 73, 75	GND	System Ground	
2, 4, 12, 14, 16, 18, 70, 72, 74	+3.3V_SB	+3.3 V Standby Voltage	
5, 7, 10, 11, 13, 17, 19, 23, 25, 29, 31, 38, 56, 58, 68, 69	NC	Not Connected	
6, 8, 20, 22, 24, 26, 28, 30	+3.3V	+3.3 V System Voltage	
32, 34, 36, 40, 42, 44, 46, 48, 67	+1.5V	+1.5 V System Voltage	
35	LPC_AD0	LPC Bus Address / Data 0	
37	LPC_AD1	LPC Bus Address / Data 1	
41	LPC_AD2	LPC Bus Address / Data 2	
43	LPC_AD3	LPC Bus Address / Data 3	
47	LPC_FRAMEn	LPC Bus Frame	
50	PLTRSTn	Platform Reset	
54	SERIRQ	Serial Interrupt Request	
55	LPC_CLK	LPC Bus 33 MHz Clock	

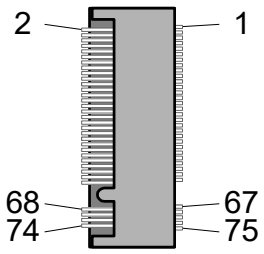


Figure 14: MPL AGs TPM Module Socket Connector (TE, TE12199230-6)

3.3.2.5 SATA 3.0 Signal Connectors (J26, J25)

Shrouded SATA connectors with up to 600 MB/s data transfer rate.

Pin	Signal	Description	Pin Assignment
1	GND	Ground	
2	SATA4/5_A+	SATA 3.0 Port 4/5 Differential Signal Pair A	
3	SATA4/5_A-		
4	GND	Ground	
5	SATA4/5_B-	SATA 3.0 Port 4/5 Differential Signal Pair B	
6	SATA4/5_B+		
7	GND	Ground	

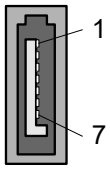


Figure 15: SATA Connector (Molex, 67800-8125)

3.3.2.6 SATA Power Connectors (J27)

Shrouded 2.54 mm header with latch.

Pin	Signal	Description	Pin Assignment
1	+5V_SATA4	Switched 5 V Power for SATA Port 4	
2	+5V_SATA5	Switched 5 V Power for SATA Port 5	
3	GPn0/2	SATA Device Detection at Port 0/2	
4	GND	Ground	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GPn1/3	SATA Device Detection at Port 1/3	
9	+3.3V_SATA5	Switched 3.3 V Power for SATA Port 5	
10	+3.3V_SATA4	Switched 3.3 V Power for SATA Port 4	

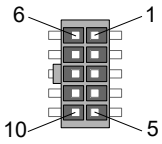


Figure 16: Power Connector for SATA Devices (Samtec, IPL1-105-02-S-D)

3.3.2.7 CMOS Backup Battery Connector (J28)

Shrouded 1.00 mm header with friction lock. Note, this connector got rotated 180° from PCB rev. A to rev. B.

Pin	Signal	Signal Description	Pin Assignment
1	VCC_Bat	Dedicated 3V Battery Input	
2	VCC_Var	Variable 2.5V to 5V Battery Input	
3	GND	Ground	

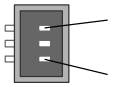


Figure 17: Backup Battery Connector (Molex, 501331-0307)

3.3.2.8 LED Indicator Panel Connector (J32)

Shrouded 1.00 mm header with positive lock used to connect MPL AGs SerLED-x module.

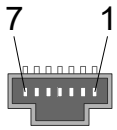
Pin	Signal	Description	Pin Assignment
1	RSTBTN	Reset Button	
2	PWRBTN	Power Button	
3	LED_DATA	Serial Data	
4	LED_GATE	Gate	
5	LED_CLOCK	Clock	
6	+3.3V	+3.3 V System Voltage	
7	GND	Ground	

Figure 18: LED Indicator Panel Connector (Molex, 501331-0707)

3.3.2.9 PEG Port Connector (J33)

For detailed information please refer to the PCI Express Base Specification 3.0 and the PCI Express CEM Specification 3.0.

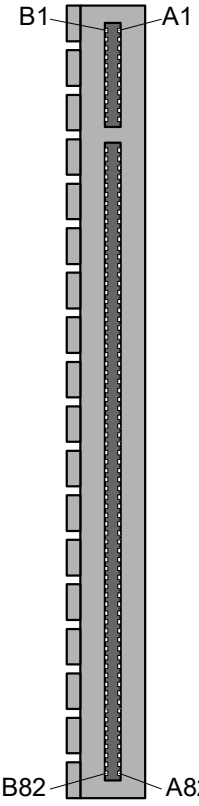
Pin	Signal	Signal Description	Pin Assignment
A1, A4, A12, A15, A18, A20, A23, A24, A27, A28, A31, A34, A37, A38, A41, A42, A45, A46, A49, A51, A54, A55, A58, A59, A62, A63, A66, A67, A70, A71, A74, A75, A78, A79, A82, B4, B7, B13, B16, B18, B21, B22, B25, B26, B29, B32, B35, B36, B39, B40, B43, B44, B47, B49, B52, B53, B56, B57, B60, B61, B64, B65, B68, B69, B72, B73, B76, B77, B80	GND	System Ground	
A2, A3, B1, B2, B3	+12V	+12 V System Voltage	
A9, A10, B8	+3.3V	+3.3 V System Voltage	
B10	+3.3V_SB	+3.3 V Standby Voltage	
A5, A6, A7, A8, A19, A32, A33, A50, B9, B12, B17, B30, B31, B48, B81, B82	NC	Not Connected	
A11	PE_RSTn	PCI Express Bus Reset	
A13, A14	PEx16_Clkp/n	PCI Express x16 Lane Clock	
A16, A17, A21, A22, A25, A26, A29, A30, A35, A36, A39, A40, A43, A44, A47, A48, A52, A53, A56, A57, A60, A61, A64, A65, A68, A69, A72, A73, A76, A77, A80, A81	PEx16_xRp/n	PCI Express x16 Lane Receive	
B5	SMB_SCL	SM Bus Clock	
B6	SMB_SDA	SM Bus Data	
B11	WAKEn	PCI Express Bus Wake	
B14, B15, B19, B20, B23, B24, B27, B28, B33, B34, B37, B38, B41, B42, B45, B46, B50, B51, B54, B55, B58, B59, B62, B63, B66, B67, B70, B71, B74, B75, B78, B79	PEx16_xTp/n	PCI Express x16 Lane Transmit	

Figure 19: PCIe PEG Port Connector (Samtec, PCIE-164-02-F-D-EMS2-BG)

3.3.2.10 PCIe/104 Interface Type 1 Connector (J34)

For detailed information please refer to the PCIe/104 Specification Version 3.0. Note, the MXCS supports a PCIe x8 lane link and not the full PCIe x16 lane link.

Pin	Signal	Signal Description	Pin Assignment
CPP1, CPP2	+5V	+5 V System Voltage	
CPP3	+12V	+12 V System Voltage	
9, 10, 15, 16, 21, 22, 27, 28, 33, 34, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80 ,85, 86, 91, 92, 97, 98, 103, 104, 107, 108, 113, 114, 119, 120, 125, 126, 131, 132, 137, 138, 143, 144, 149, 150, 155, 156	GND	System Ground	
1	*USB_OCn*	*USB Ports Over Current* *1	
2	PE_RSTn	PCI Express Bus Reset	
3, 4	+3.3V	+3.3 V System Voltage	
5, 7	USB_1+/-	USB 2.0 Port Balanced Data Line	
6, 8	USB_0+/-	USB 2.0 Port Balanced Data Line	
11, 13	PEx1_1Tp/n	PCI Express x1 Lane Port 1 Transmit	
12, 14	PEx1_0Tp/n	PCI Express x1 Lane Port 0 Transmit	
17, 19	PEx1_2Tp/n	PCI Express x1 Lane Port 2 Transmit	
18, 20	PEx1_3Tp/n	PCI Express x1 Lane Port 3 Transmit	
23, 25	PEx1_1Rp/n	PCI Express x1 Lane Port 1 Receive	
24, 26	PEx1_0Rp/n	PCI Express x1 Lane Port 0 Receive	
29, 31	PEx1_2Rp/n	PCI Express x1 Lane Port 2 Receive	
30, 32	PEx1_3Rp/n	PCI Express x1 Lane Port 3 Receive	
35, 37	PEx1_1Clkp/n	PCI Express x1 Lane Port 1 Clock	
36, 38	PEx1_0Clkp/n	PCI Express x1 Lane Port 0 Clock	
39, 40	+5V_SB	+5V Standby Voltage (Active in ATX S5 State)	
41, 43	PEx1_2Clkp/n	PCI Express x1 Lane Port 2 Clock	
42, 44	PEx1_3Clkp/n	PCI Express x1 Lane Port 3 Clock	
45	GND (DIR)	Ground, Indicates that the PCIe Connector is on the Top Side of the MXCS PCB	
46	PWRGOOD	Power Good	
47, 49, 51	SMBus	SM Bus Data, Clock and Alert	
48, 50	PEx16_Clkp/n	PCI Express x16 Lane Clock (PEG Port)	
52	PSONn	Power Supply On Output (Low Active) (Reserved for MPL AG only Use)	
53	WAKEn	PCI Express Bus Wake	
54	PEG_ENAn	PCI Express Graphics (PEG) Device Enable	
58, 60, 64, 66, 70, 72, 76, 78, 82, 84, 88, 90, 94, 96, 100, 102	PEx8_xTp/n	PCI Express x8 Lane Transmit (PEG Port)	
105, 106	SDVO	SDVO not used (100k Pull Down)	
110, 112, 116, 118, 122, 124, 128, 130, 134, 136, 140, 142, 146, 148, 152, 154	PEx8_xRp/n	PCI Express x8 Lane Receive (PEG Port)	
57, 59, 63, 65, 69, 71, 75, 77, 81, 83, 87, 89, 93, 95, 99, 101, 109, 111, 115, 117, 121, 123, 127, 129, 133, 135, 139, 141, 145, 147, 151, 153	*PEx16_xXp/n*	*The remaining and not supported PCI Express x16 lane link signals are not connected.* *1	

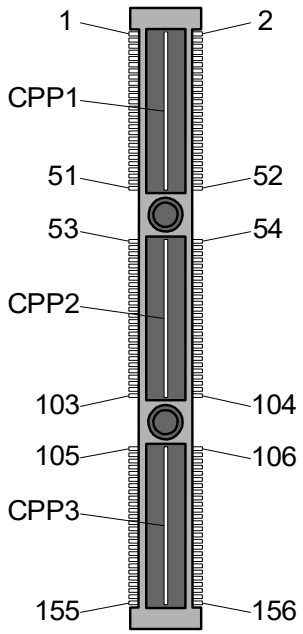


Figure 20: PCIe/104 Connector (Samtec, ASP-129637-03)

Note:

*1: All the grayed out signals are not connected and therefore not used and not available at the MXCS.

3.3.2.11 mPCIe Full-Mini Card Sockets 0 – 3 (J38, J41, J44, J46)

These sockets support mPCIe Full-Mini Card modules according to PCI Express Mini Card Electromechanical Specification Revision 2.0.

Pin	Signal	Pin	Signal
1	WAKEn	2	+3.3V
3	Not Connected	4	GND
5	Not Connected	6	+1.5V
7	CLKREQn	8	SIM_PWR *1
9	GND	10	SIM_DATA *1
11	REFCLK-	12	SIM_CLK *1
13	REFCLK+	14	SIM_RSET *1
15	GND	16	SIM_VPP *1
17	Not Connected	18	GND
19	Not Connected	20	W_DISABLEn
21	GND	22	PE_RSTn
23	PERn	24	+3.3V
25	PERp	26	GND
27	GND	28	+1.5V
29	GND	30	Not Connected
31	PETn	32	Not Connected
33	PETp	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V	40	GND
41	+3.3V	42	LED_WWANn
43	GND	44	LED_WLANn
45	Not Connected	46	LED_WPANn
47	Not Connected	48	+1.5V
49	Not Connected	50	GND
51	Not Connected	52	+3.3V

Pin Assignment

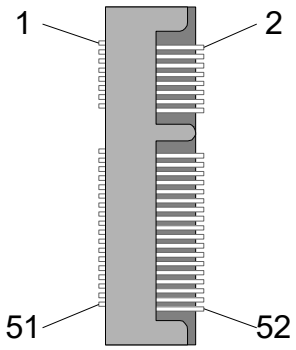


Figure 21: mPCIe Full-Mini Card Socket Connector (JAE, MM60-52B1-E1-R650)

Note:

*1: J44 and J46 don't support the SIM card interface.

3.3.2.12 mPCIe Socket 0 and 1 SIM Card Connectors (J39, J42)

This connectors support MPL AGs SIMext-1 Mini-SIM card adapter.

Pin	Signal	Description
1	VCC	Power Supply Input
2	RESET	Reset Signal
3	CLK	Clock Signal
4	GND	Ground
5	VPP	Programming Voltage Input
6	I/O	Serial Data Input/Output

Pin Assignment

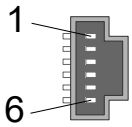


Figure 22: SIM Card Connector (Molex, 501331-0607)

3.3.2.13 mPCIe Socket 0 – 3 WLAN Disable Connector (J40, J43, J45, J47)

The mPCIe socket WLAN Disable signal is available at a solder pad.

Pin	Signal	Description
1	GND	Ground
2	W_DISABLExn	mPCIe Socket 1 WLAN Disable Signal (Connect to GND for Disabling)

Pin Assignment

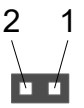


Figure 23: WLAN Disable Solder Pads

3.3.2.14 Fan Connector (J49)

This connector is reserved for the MXCS fan solution.

Pin	Signal	Description
1	FAN_PWM	Fan PWM Speed Control Signal
2	FAN_TACHO	Fan PWM Revolution Control Signal
3	FAN_PRESENCEn	FAN Module Presence Signal
4	GND	Ground
5	+5V	+5 V System Voltage
6	GND	Ground
7	+12V	+12 V System Voltage
8	GND	Ground
9	+12V	+12 V System Voltage
10	GND	Ground

Pin Assignment

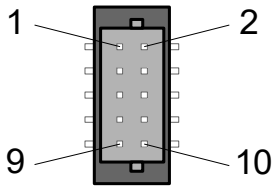


Figure 24: Fan Connector (Hirose, DF11CZ-10DS-2V)

3.3.2.15 MXCS USB Sub Module Connector (J14)

This connector is used to connect the MXCS USB sub module.

3.3.2.16 MXCS Serial Port Sub Module Connector (J15)

This connector is used to connect the MXCS Serial Port sub module.

3.3.2.17 MXCS Ethernet Sub Module Connector (J36)

This connector is used to connect the MXCS Ethernet sub module.

3.3.2.18 MXCS IPMI BMC Sub Module Connector (J37)

This connector is used to connect the MXCS IPMI BMC sub module.

3.3.2.19 Serial Debug Connector (J3)

This connector is reserved for MPL AG test purpose.

3.3.2.20 Intel XDP Connector (J4)

This connector is reserved for MPL AG test purpose.

3.3.2.21 Write Protect Jumper (J9)

This connector is reserved for MPL AG production purpose.

3.3.2.22 I^2C Port Connector (J16)

This connector is reserved for MPL AG production purpose.

3.3.2.23 Port80 Connector (J30)

This connector is reserved for MPL AG test purpose.

3.3.2.24 JTAG Port Connector (J31)

This connector is reserved for MPL AG production purpose.

3.4 MODULE SOCKETS

3.4.1 MEMORY MODULES

3.4.1.1 Electrical and Mechanical Requirements

Four memory module sockets with JEDEC standard layout support DDR4-2400 (PC4-19200) 288 pin unbuffered DIMM (UDIMM) or registered DIMM (RDIMM) modules. UDIMMs are supported up to 16GiB (with 8Gibit chips), RDIMMs up to 32 GiB (with 8 GiBit chips).
The memory modules listed bellow are tested and approved. Regarding the special environmental conditions the MXCS is normally used, MPL AG recommends to use low power industrial type memory modules.
It is the customers responsibility that memory modules supplied by third party vendors meet the above stated requirements. MPL AG will not be liable for memory modules that are purchased from third party vendors and don't work in the MXCS.

Module Manufacturer	Part Number	Description
InnoDisk	M4R0-BGS3GCSJ	32 GiB, ECC RDIMM, DDR4-2400 CL-17-17-17-39
Kingston	HX424C15FBK4/16	4 GiB, NonECC UDIMM, DDR4-2400 CL15-15-15
Kingston	KVR21R15S8/4	4 GiB, ECC RDIMM, DDR4-2133 CL15-15-15
Kingston	KVR24R17D4/32	32 GiB, ECC RDIMM, DDR4-2400 CL17-17-17
Memphis	D4RV1G724GI-A18SB	8 GiB, ECC RDIMM, DDR4-2400 CL
Memphis	D4RV2G724GI-A18SB	16 GiB, ECC RDIMM, DDR4-2400 CL
Samsung	ECCM393A4K40CB1-CRC	32 GiB, ECC RDIMM, DDR4-2400 CL-17-17-17-39

3.4.1.2 Mounting the Memory Modules

Please be careful with the bare memory modules. Electrostatic discharge is a destructive issue to all of its electronic components.
If you use only one memory module, populate channel 0 DIMM 0. If you use two memory modules, additionally populate CH1 DIMM0. If you do otherwise, it is possible that the MXCS will not boot.
Note, it is not possible to mix UDIMM and RDIMM modules. If you do so, the MXCS will not boot.

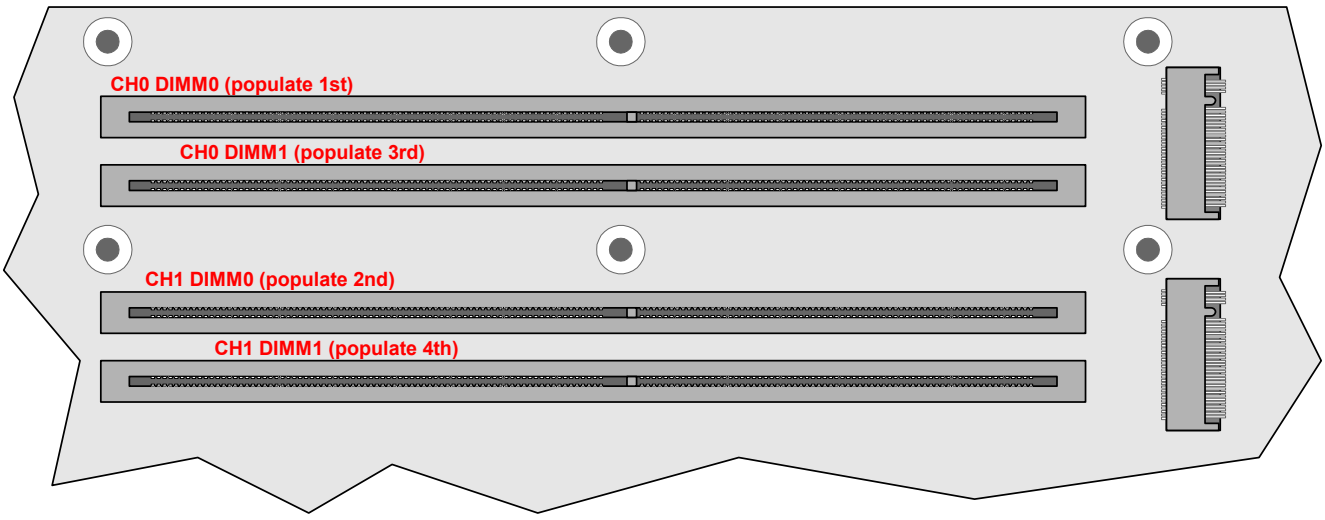


Figure 25: Mounting the DIMMs

3.4.2 PCIe/104 TYPE 1 STACK

There is a PCIe/104 Type 1 slot available with one PCIe Gen3 x8 lane link, four PCIe Gen2 x1 lane links and two USB 2.0 interfaces.
Please follow the appropriate module user manuals for installing and setup the PCIe/104 modules.

3.4.3 mPCIe SOCKETS

There are four mPCIe Full-Mini Card sockets available, two of them with SIM card support, to expand the MXCS with various IO interfaces (like LAN, WLAN, GSM, GPRS, UMTS, DVB-T, Frame Grabber, CAN, IEEE1394 A+B, ..).

These sockets support the PCI Express Mini Card Electromechanical Specification Revision 2.0. The sockets are not powered in the S5 power state. The pin out can be found in chap. 3.3.2.11.
Please follow the appropriate module user manuals for installing and setup the several add-on modules.

3.4.4 M.2 SOCKETS

There are two M.2 Key M sockets available to expand the MXCS with M.2 Solid State Disks. The M.2 slots support 42 mm, 60 mm and 80 mm modules with SATA 3.0 interface. The PCIe interface is not supported at the M.2 slots.

3.4.5 mSATA SOCKETS

There are two mSATA sockets available to expand the MXCS with mSATA Solid State Disks. The mSATA slots support mSATA modules with SATA 3.0 interface.

3.4.6 SFP+ MODULES

There are two SFP+ cages available to expand the MXCS with up to two 10 GbE interfaces.
The SFP+ modules listed bellow are tested and approved.

Module Manufacturer	Part Number	Description
Broadcom Avago	AFBR-5710APZ	1.25 Gbps, 1000Base-SX, 850 nm multi-mode
Fiberstore	SFP-10GLR-31	10.3125 Gbps, 10GBase-LR, 1310 nm single-mode
Fiberstore	SFP-10GSR-85	10.3125 Gbps, 10GBase-SR, 850nm multi-mode
Finisar	FTLR1471D3BNL	10.3125 Gbps, 10GBase-LR, 1310nm single-mode
Finisar	FTLX8573D3BTL	10.3125 Gbps, 10GBase-SR, 850nm multi-mode
Intel	FTLX8571D3BCV-I3	1.25 Gbps / 10.3125 Gbps dual rate, 1000Base-SX / 10GBase-SR/SW, 850 nm, multi-mode
Supermicro	CBL-0348L	10 Gbps Twinax DAC cable

3.5 SYSTEM-VOLTAGES SUPPLIED BY THE MXCS

The MXCS has the ability to supply +3.3 V, +5 V, the related standby voltages +3.3 V_SB and +5 V_SB and +12 V to several connectors on the MXCS PCB. But there are some specialties to pay attention to about this voltage rails:

- The current capability is limited on all the supplied system voltages.
- These voltages are not fused on the internal connectors. So a short circuit may cause an immediate shutdown or even serious damage to the MXCS PCB or its components.

On the MXCS there is one switching regulator that supplies power to the +3.3 V_SB power rail directly and via a MOSFET switch it supplies power to the +3.3 V power rail also. The same at +5 V, one switching regulator for both the +5.0 V_SB and the +5.0 V power rail. Each switching regulator supplies maximum 15 A to their related 3.3 V(_SB) or 5.0 V(_SB) loads.
The +12 V_SB switching regulator supplies its power to the +12 V and to the 3.3V_SB and the 5V_SB switching regulators. So the total power used at all these voltage rails must not exceed the capability of the +12 V_SB switching regulator.

Voltage	Possible Loads	Maximum Current (Power)
+3.3 V_SB	- SFP+ cages (J10, J12) - TPM socket (J29) - PEG port (J33) - +3.3 V voltage rail (see below)	15 A (50 W)
+3.3 V	- M.2 sockets (J18, J20) - mSATA sockets (J21, J23) - SATA Power (J27) - TPM socket (J29) - PEG port (J33) - PCIe/104 stack (J34) - mPCIe sockets (J38, J41, J44, J46)	
+5.0 V_SB	- PCIe/104 stack (J34) - +5.0 V voltage rail (see below)	15 A (75 W)
+5.0 V	- SATA Power (J27) - PCIe/104 stack (J34) - FAN connector (J49) - USB ports 1-4	
+12 V_SB	- +3.3 V_SB switching regulator - +5.0 V_SB switching regulator - +12 V voltage rail (see below)	15 A (180 W)
+12 V	- PEG port (J33) - PCIe/104 stack (J34) - FAN connector (J49)	

4 THEORY OF OPERATION

4.1 BLOCK DIAGRAM

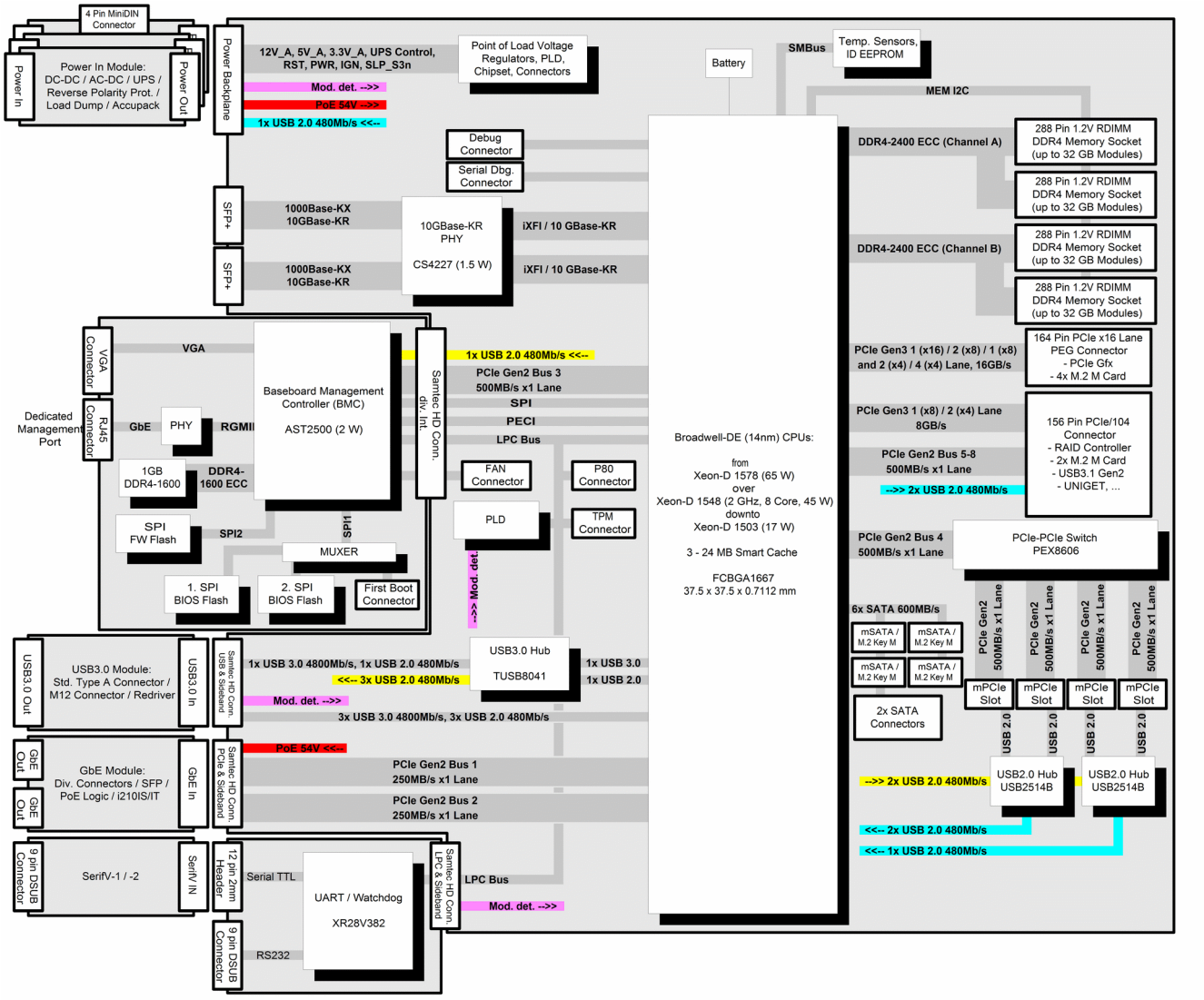


Figure 26: Complete MXCS Block Diagram

Note:

- There are many differently equipped MXCS variants available in many different housings. Please refer to your ordering and to the appropriate Operators Quick Reference Manual to see all the available features.

4.2 STATUS INDICATORS

The MXCS provides 3 status indicator LEDs at the front plate and 4 status indicator LEDs at the Ethernet connectors, giving you visual information about the actual operating status.

Indicator LED	Meaning	
Power Input LED	Red: Green:	Power Input is below 8 V. Power Input is above 8 V.
Power LED	Dark: Orange: Green: Green / orange blinking: Orange / red blinking:	MXCS in ACPI power state G3 (Mechanical OFF) MXCS in ACPI power state S5 (Soft Off) MXCS in ACPI power state S0 (Working) CPU temperature > 105 °C MXCS in ACPI power state S5, because CPU temperature was > 125 °C (immediate shutdown for CPU thermal protection) *1
Reset LED	Red: Red blinking:	MXCS in reset state Power failure detected, please turn off the power supply feeding the MXCS and remove the power failure issue.
LAN [1..2] Activity LED	Dark: Green: Green blinking:	No link Link detected Link with activity
LAN [1..2] Speed LED	Dark: Green: Orange:	No link or 10 Mbit/s link 100 Mbit/s link 1 Gbit/s link

Note:
*1: Please let the MXCS cool down first and then check the cooling system against any defects.

4.3 BATTERY CIRCUIT

Battery type: Renata CR2032 3 V / 230 mAh Lithium Coin Cell (20 x 3.2 mm)

An on board battery provides power to the Real Time Clock (RTC) and the CMOS RAM circuit.
The battery holder is an easy release type.

4.4 WATCHDOG TIMER

The watchdog timer is available with the MXCS Serial Port sub module. The sub module provides the XR28V382 UART watchdog timer with a programmable granularity of 10 ms, 1 s or 1 minute. That results in a timeout from 2.5 seconds up to 4 hours. The watchdog timer does a system reset if the timeout has expired.

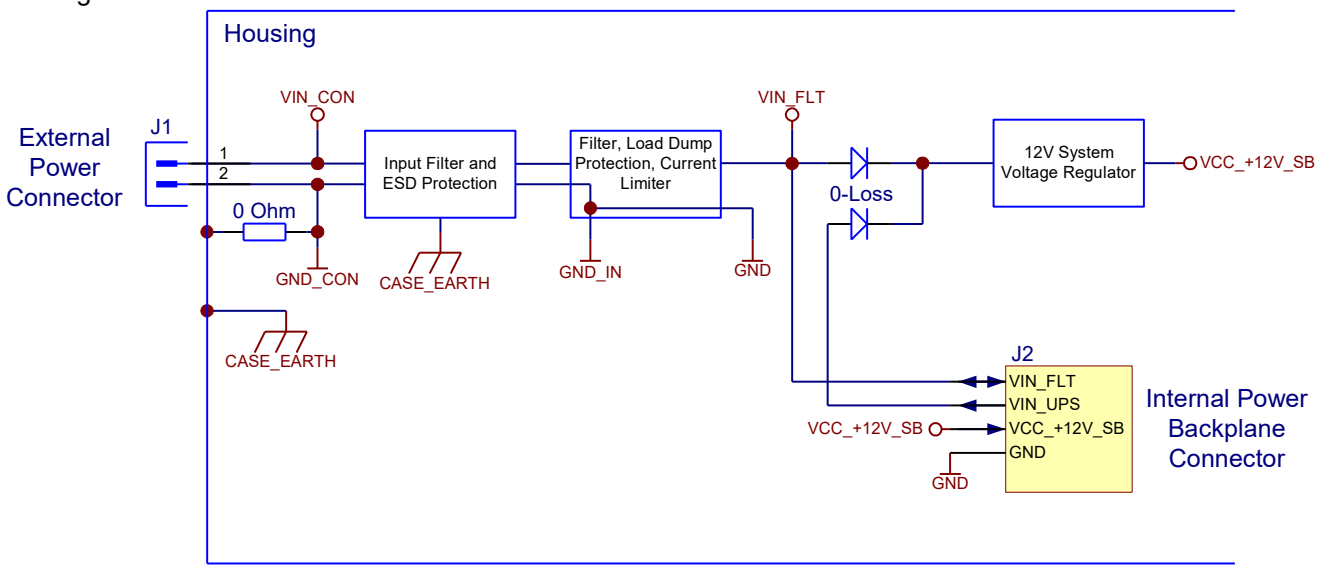
4.5 TEMPERATURE SENSORS

For monitoring the system health there are several temperature sensors available at the MXCS.

Temperature	Sensor Type	Interface and Address
CPU, individual core	Intel CPU Digital Thermal Sensors (DTS)	CPU MSR register block
Memory, DIMM modules	Type and availability depends on memory module	Memory I^2C bus
Motherboard, near power input circuit	LM75	SMBus: Addr = $48 (7 bit)
Motherboard, centric	LM75	SMBus: Addr = $49 (7 bit)

4.6 EARTHING AND GALVANIC ISOLATION

The MXCS is designed to support different earthing schemes. Please refer to the electrical schematics below, to understand the different possibilities. In this chapter it is assumed that the MXCS is well earthed over its housing.



4.6.1 DESKTOP PC EARTHING SCHEME (MXCS DEFAULT)

The Power Input, the housing and all the interfaces are referenced to CASE_EARTH. That means GND_CON, GND_IN and GND are shorted to CASE_EARTH. This earthing scheme is Desktop PC compatible and is the default MXCS earthing scheme.

Pros	Cons
• Everything is as normal as with a desktop PC. • Standard PC periphery can be used without constraints.	• Ground loops are possible. • A wrong polarized earthed power supply or one with a potential difference between earth and its negative pole induces a short circuit current via GND_CON to CASE_EARTH and on earth back to the power supply. • This may damage the MXCS GND_CON → CASE_EARTH path or the used power supply.

4.6.2 GALVANICALLY ISOLATED HOUSING (OPTIONAL)

With this earthing scheme the connection between CASE_EARTH and GND_CON is replaced with a 10 MΩ resistor.

Pros	Cons
• The ground loop “power supply ↔ MXCS” is opened, no current flow on earth. • A wrong polarized earthed power supply or one with a potential difference between earth and its negative pole doesn't damage the MXCS (if the ground loop isn't closed again with external hardware).	• It is easily overlooked that external PC hardware like USB flash drives or PC monitors often short again the connection between CASE_EARTH and the ground (GND) pins of the appropriate interface connectors (USB, DVI, …). • Then all the ground loop current (e.g. from a wrong polarized earthed power supply) flows through the GND and signal pins of the appropriate interface connector and through the external connected hardware to earth and back to the power supply. • A wrong polarized high output power supply then may damage the external hardware and the corresponding MXCS interface.

4.6.3 GALVANICALLY ISOLATED HOUSING AND POWER INPUT (OPTIONAL)

With this earthing scheme the connection between CASE_EARTH and GND_CON is replaced with a 10 MΩ resistor. Additionally a galvanically isolated DC/DC Converter with its own external power connector supplies VIN_FLT via the internal power backplane connector.

Pros	Cons
• The ground loop “power supply ↔ MXCS” is opened two times, no current flows on earth. • A wrong polarized earthed power supply doesn't damage the MXCS. • An electrical potential difference between the power supply and the MXCS doesn't damage the MXCS or possibly connected external PC hardware.	• Also with this configuration ground loops are possible. • External PC hardware may short the connection between CASE_EARTH and the GND pins of the appropriate interface connector. • Also shielded cables like some Ethernet cables may short CASE_EARTH to a far away earthed Ethernet switch.

4.6.4 CONCLUSION

If the MXCS is used in a wide branched system of power supply, external connected devices or Ethernet lines it is important to understand where closed ground loops are, where voltages can be coupled into this system, where an electrical potential difference may occur and what may happen if something goes wrong or is wrongly connected.
In this regard at risk are MXCS, which are mounted near heavy electrical loads, near electrical drives, at vehicles or at wide branched industrial facilities.
The needed earthing scheme and potential other precautions heavily depend on the electrical environment the MXCS is used in.

5 SOFTWARE

5.1 MXCS EXTENSION REGISTER SET

5.1.1 OVERVIEW

IO-Address	Function	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$800	Serial Ports Status Register	Reserved	Reserved	*SER4_STS1*	*SER4_STS0*	Reserved	Reserved	*SER3_STS1*	*SER3_STS0*
$801	Boot LED Register	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	*BLED_RD*	*BLED_GN*
$802	SATA Power Register	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	*SATA_PEN1*	*SATA_PEN0*
$803	Ignition Pin Configuration Register	*PBTN_OVR*	*IGNITION*	*IGN_TOUT5*	*IGN_TOUT4*	*IGN_TOUT3*	*IGN_TOUT2*	*IGN_TOUT1*	*IGN_TOUT0*
$804	USB Module Configuration	Reserved	Reserved	Reserved	Reserved	*USB_PRE3*	*USB_PRE2*	*USB_PRE1*	*USB_PRE0*
$805	VIN Module Present	Reserved	Reserved	Reserved	Reserved	*VIN_PRE3*	*VIN_PRE2*	*VIN_PRE1*	*VIN_PRE0*
$806	VIN Module Power OK	Reserved	Reserved	Reserved	Reserved	*VIN_POK3*	*VIN_POK2*	*VIN_POK1*	*VIN_POK0*
$807	RESERVED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$808	ACPI BIOS scratch Register	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)	Reserved (do not modify)
$809	User LED Control Register	Reserved	Reserved	Reserved	Reserved	*ULED2_RD*	*ULED2_GN*	*ULED1_RD*	*ULED1_GN*
$80A	MXCS Status Register	*WLAN3_DIS*	*WLAN2_DIS*	*WLAN1_DIS*	*WLAN0_DIS*	Reserved	Reserved	*NIC1_DIS*	*NIC0_DIS*
$80B	RESERVED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$80C	RESERVED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
$80D	MXCS PCB Revision Register	Reserved	Reserved	Reserved	Reserved	*PCB_REV3*	*PCB_REV2*	*PCB_REV1*	*PCB_REV0*
$80E	PLD Code ID Register	*PLD_ID7*	*PLD_ID6*	*PLD_ID5*	*PLD_ID4*	*PLD_ID3*	*PLD_ID2*	*PLD_ID1*	*PLD_ID0*
$80F	PLD Code Revision Register	*PLD_REV7*	*PLD_REV6*	*PLD_REV5*	*PLD_REV4*	*PLD_REV3*	*PLD_REV2*	*PLD_REV1*	*PLD_REV0*

5.1.2 SERIAL PORTS STATUS REGISTER

Address: IO 800h
Default Value: 00xx'00xxb
Access: Read only

Bit	Access	Default Value	Description
7:6	RO	00b	**Reserved**
5:4	RO	xxb	**SER2_STS[1..0]:** These bits report the serial port 2 interface type.
			Encoding: 00b – Reserved; 01b – RS232; 10b – RS422 / RS485; 11b – Interface not used
3:2	RO	00b	**Reserved**
1:0	RO	xxb	**SER1_STS[1..0]:** These bits report the serial port 1 interface type.
			Encoding: 00b – Reserved; 01b – RS232; 10b – RS422 / RS485; 11b – Interface not used

5.1.3 BOOT LED REGISTER

Address: IO 801h
Default Value: 00h
Access: Read only, Read / Write

Bit	Access	Default Value	Description
7:2	RO	0000'00b	**Reserved**
1:0	RD / WR	00b	**BLED_RD/GN:** These bits define the Boot LED status.
			Encoding: 00b – Boot LED Off; 01b – Boot LED lights green; 10b – Boot LED lights red; 11b – Boot LED lights orange (green and red)

5.1.4 SATA POWER REGISTER

Address: IO 802h
Default Value: 00h
Access: Read only, Read / Write

Bit	Access	Default Value	Description
7:2	RO	0h	**Reserved**
1	RD / WR	1b	**SATA_PEN1:** This bit defines the SATA port 1 power state.
			Encoding: 0b – +3.3V/+5V_SATA1 Power Off; 1b – +3.3V/+5V_SATA1 Power On
0	RD / WR	1b	**SATA_PEN0:** This bit defines the SATA port 0 power state.
			Encoding: 0b – +3.3V/+5V_SATA0 Power Off; 1b – +3.3V/+5V_SATA0 Power On

5.1.5 IGNITION PIN CONFIGURATION REGISTER

There is a short time at boot up while the operating systems do not proper detect an ignition (or also a power button) shutdown command. WIN7 do even a blue screen, if the shutdown command is issued to early.
So the IGN_TOUT timeout can be used to span this time which the OS needs to fully boot up and then proper detect an ignition event.

Address: IO 803h
Default Value: 0x00'0100h
Access: Read only, Read / Write

Bit	Access	Default Value	Description
7	RD / WR	0b	**PBTN_OVR:** This bit defines if a Power Button Override will be executed if the MXCS do not proper shut down after the Ignition Signal goes low.
			Encoding / **Description** 0b / Do Nothing 1b / Do a PWR Button Override after 30 seconds
6	RO	xb	**IGNITION:** This bit reports the status of the IGNITION signal.
			Encoding / **Description** 0b / IGNITION signal is LOW. 1b / IGNITION signal is HIGH.
5:0	RD / WR	4h	**IGN_TOUT:** This bits define the Ignition Pin Timeout in seconds between a fresh MXCS power up from power state S5 and the first time an ignition pin event will be executed. So a MXCS do not shut down before this timeout is matured. The ignition pin transition will be buffered during this time.
			Encoding / **Description** 0h / No Timeout 4h / 4 s Timeout (default) ... / up to 63 s Timeout

5.1.6 USB MODULE PRESENCE REGISTER

Address: IO 804h
Default Value: 0xh
Access: Read only

Bit	Access	Default Value	Description
7:4	RO	0000b	**Reserved**
3:2	RO	xxb	**USB_PRE[3..2]:** This bit reports if USB ports 2 and 3 are present.
			Encoding / **Description** 00b / Reserved 01b / Type A connector Super Speed ports 10b / Reserved 11b / USB ports not present
1:0	RO	xxb	**USB_PRE[1..0]:** This bit reports if USB ports 0 and 1 are present.
			Encoding / **Description** 00b / Reserved 01b / Type A connector Super Speed ports 10b / Reserved 11b / USB ports not present

5.1.7 VIN MODULE PRESENCE REGISTER

Address: IO 805h
Default Value: 0xh
Access: Read only

Bit	Access	Default Value	Description
7:4	RO	0000b	**Reserved**
3	RO	xb	**VIN_PRE3:** This bit reports if the V_{IN} Module 3 is present. **Encoding** / **Description** 0b: V_{IN} Power Module present 1b: V_{IN} Power Module not present
2	RO	xb	**VIN_PRE2:** This bit reports if the V_{IN} Module 2 is present. **Encoding** / **Description** 0b: V_{IN} Power Module present 1b: V_{IN} Power Module not present
1	RO	xb	**VIN_PRE1:** This bit reports if the V_{IN} Module 1 is present. **Encoding** / **Description** 0b: V_{IN} Power Module present 1b: V_{IN} Power Module not present
0	RO	xb	**VIN_PRE0:** This bit reports if the V_{IN} Module 0 is present. **Encoding** / **Description** 0b: V_{IN} Power Module present 1b: V_{IN} Power Module not present

5.1.8 VIN MODULE POWER OK REGISTER

Address: IO 806h
Default Value: 0xh
Access: Read only

Bit	Access	Default Value	Description
7:4	RO	0000b	**Reserved**
3	RO	xb	**VIN_POK3:** This bit defines the V_{IN} Module 3 power state. **Encoding** / **Description** 0b: V_{IN} Power Not OK 1b: V_{IN} Power OK
2	RO	xb	**VIN_POK2:** This bit defines the V_{IN} Module 2 power state. **Encoding** / **Description** 0b: V_{IN} Power Not OK 1b: V_{IN} Power OK
1	RO	xb	**VIN_POK1:** This bit defines the V_{IN} Module 1 power state. **Encoding** / **Description** 0b: V_{IN} Power Not OK 1b: V_{IN} Power OK
0	RO	xb	**VIN_POK0:** This bit defines the V_{IN} Module 0 power state. **Encoding** / **Description** 0b: V_{IN} Power Not OK 1b: V_{IN} Power OK

5.1.9 ACPI BIOS SCRATCH REGISTER

Address: IO 808h
Default Value: 00h
Access: Read / Write

Bit	Access	Default Value	Description
7:0	RD / WR	00h	**Reserved** Used by the MXCS BIOS. Do not modify this register.

5.1.10 USER LED REGISTER

Address: IO 809h
Default Value: 00h
Access: Read only, Read / Write

Bit	Access	Default Value	Description
7:4	RO	0000b	**Reserved**
3:2	RD / WR	00b	**USER_LED2:** These bits define the User LED2 status.
			Encoding / **Description** 00b / User LED2 Off 01b / User LED2 lights green 10b / User LED2 lights red 11b / User LED2 lights orange (green and red)
1:0	RD / WR	00b	**USER_LED1:** These bits define the User LED1 status.
			Encoding / **Description** 00b / User LED1 Off 01b / User LED1 lights green 10b / User LED1 lights red 11b / User LED1 lights orange (green and red)

5.1.11 MXCS STATUS REGISTER

Address: IO 80Ah
Default Value: xxh
Access: Read only

Bit	Access	Default Value	Description
7	RO	xb	**WLAN3_DIS:** This bit reports the mPCIe Socket 3 radio operation disable signal.
			Encoding / **Description** 0b / mPCIe Socket 3 Radio Operation Disabled 1b / Normal Operation
6	RO	xb	**WLAN2_DIS:** This bit reports the mPCIe Socket 2 radio operation disable signal.
			Encoding / **Description** 0b / mPCIe Socket 2 Radio Operation Disabled 1b / Normal Operation
5	RO	xb	**WLAN1_DIS:** This bit reports the mPCIe Socket 1 radio operation disable signal.
			Encoding / **Description** 0b / mPCIe Socket 1 Radio Operation Disabled 1b / Normal Operation
4	RO	xb	**WLAN0_DIS:** This bit reports the mPCIe Socket 0 radio operation disable signal.
			Encoding / **Description** 0b / mPCIe Socket 0 Radio Operation Disabled 1b / Normal Operation
3:2	RO	00b	**Reserved**
1	RO	xb	**NIC2_DIS:** This bit reports the DIP switch S2-7 status.
			Encoding / **Description** 0b / NIC2 Controller Disabled 1b / NIC2 Controller Normal Operation
0	RO	xb	**NIC1_DIS:** This bit reports the DIP switch S2-8 status.
			Encoding / **Description** 0b / NIC1 Controller Disabled 1b / NIC1 Controller Normal Operation

5.1.12 MXCS PCB REVISION REGISTER

Address: IO 80Dh
Default Value: xxh
Access: Read only

Bit	Access	Default Value	Description	
7:0	RO	xxh	**PCB_REV[7..0]:** These bits report the MXCS PCB revision.	
			Encoding	**Description**
			00h	PCB Rev. A
			01h	PCB Rev. B
			02h	PCB Rev. C
			...	...

5.1.13 PLD CODE ID REGISTER

Address: IO 80Eh
Default Value: xxh
Access: Read only

Bit	Access	Default Value	Description	
7:0	RO	xxh	**PLD_ID[7..0]:** These bits report the PLD code ID.	
			Encoding	**Description**
			00h	PLD Code ID P00
			01h	PLD Code ID P01
			02h	PLD Code ID P02
			...	...

5.1.14 PLD CODE REVISION REGISTER

Address: IO 80Fh
Default Value: 0xh
Access: Read only

Bit	Access	Default Value	Description	
7:0	RO	xxh	**PLD_REV[7..0]:** These bits report the PLD code revision.	
			Encoding	**Description**
			00h	PLD Code Revision V00
			01h	PLD Code ID V01
			02h	PLD Code ID V02
			...	...

5.2 BIOS

BIOS upgrading is easily possible. Please refer to the MXCS System BIOS User Manual for additional information.
Please ask MPL support at support@mpl.ch for the latest BIOS version.

5.3 DEVICE DRIVERS

All the drivers are available at the MPL AG homepage:

https://www.mpl.ch/t5013.html

5.4 TOOLS

There are different hardware monitoring features that can be reported with several freeware tools:

- CoreTemp CPU monitor:

https://www.alcpu.com/CoreTemp/

- HWiNFO Hardware Monitor:

https://www.hwinfo.com/

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6 COPYRIGHT

7 DISCLAIMER

MPL AG has fully tested the MXCS and reviewed the documentation. However, MPL AG makes no warranty or representation, either expressed, or implied, with respect to this product, its quality, performance, merchantability, or fitness for a particular purpose.
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8 TRADEMARKS

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9 SUPPORT

9.1 FAQs

Please have a look at the homepage www.mpl.ch/t5000.html. In the menu at the left hand side you will find FAQ's for each available MXCS.

9.2 SERIAL NUMBER AND REVISION

When contacting MPL Support it is important that you declare the MXCS type, the serial number with revision and the BIOS number. Please have a look at the label on the MXCS housing for this.

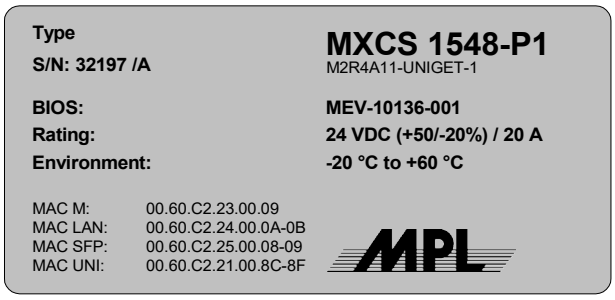

Figure 27: MXCS Label

9.3 CONTACTING MPL AG

In case of general questions please feel free to contact MPL AG at the homepage (www.mpl.ch) or per email (info@mpl.ch).
In case of sales questions please send your email to sales@mpl.ch.
If you have a technical problem with a MXCS, first please carefully read the BIOS user manual, this manual and the FAQs at the homepage. If you can't solve the problem on your own, you can contact MPL AG for technical support per email at support@mpl.ch.

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